AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows:

Please replace paragraphs [0004], [0012], [0013], [0017], [0018], [0022]-[0024], [0027] and [0028] with the following amended paragraphs:

[0004] Thermal epoxy has heat transfer limitations that impede efficient heat transfer from the die. Although solder has better heat transfer properties than thermal epoxy, it requires metallization, such the deposition of metal as a thin layer of gold, on the back side of the die, as indicated by layers 150 in Fig. 1B. In addition, in both the thermal epoxy alternative and the solder alternative, heat is transferred from the package essentially through ~~a layer of dielectric as~~ the processor substrate, such as silicon. However, silicon is a poor thermal conductor, typically having a thermal conductivity of 148 W/m/K. Disadvantageously, the heat spreader in both of the attachment schemes described above requires a heat spreader to be attached to the die with a relatively large amount of silicon, for example, a silicon layer having a thickness between about 5 to about 200 microns, disposed between the heat spreader and the circuit generating the heat.

[0012] Fig. 5 is a schematic view similar to Fig. 2 showing a silicon layer as having been disposed on the layer of copper of Fig. 4 to provide a

~~dielectric~~-thermal conductor sandwich, according to an embodiment of the present invention;

[0013] Fig. 6 is a schematic view similar to Fig. 2 showing an intermediate die built up according to any one of standard manufacturing processes and incorporating the ~~dielectric~~-thermal conductor sandwich shown in Fig. 5 according to an embodiment of the present invention;

[00017] Embodiments of the present invention contemplate the inclusion of a thermally conductive material, such as copper, in an inner region of a microelectronic die for effecting heat dissipation from the inner region of the die through the thermally conductive material and away from the die. By "microelectronic die," what is meant is a microelectronic package including a microelectronic circuit, such as a microprocessor. As is well known, microelectronic ~~dies~~ dice generate heat when being operated. The thermally conductive material in the inner region of the die draws the heat away from the microelectronic circuit, according to embodiments of the present invention. The thermally conductive material may comprise a copper layer, but any other suitable thermal conductor can be used, as recognized by one skilled in the art. The heat dissipation would take place through the copper layer and through thermal contact zones comprising copper connections to a heat spreader attachment mechanism. The efficiency of the heat transfer process from a die packaged according to

embodiments of the present invention is increased relative to dies packaged according to the prior art. Embodiments of the present invention use a thermally conductive material, such as copper, to draw heat from the inner region of the die and to transfer it away from the die, such as to a heat spreader, thus improving the overall heat transfer characteristics of the package. The heat transfer from the inner region of the die to the heat spreader may be effected through thermal contact zones that include copper filled thermal vias, and thereafter may be effected through solder, to a heat spreader. Embodiments of the present invention advantageously allow higher processor speeds by improving heat dissipation from microelectronic dies. By way of example, where copper is used as the thermally conductive material in the inner region of the die, there would be approximately a threefold increase in the heat dissipation from the die with respect to dies relying solely on ~~a dielectric~~ the wafer material, such as silicon for the dissipation of heat.

[0018] Turning now to the drawings, Figs. 2-7 depict various stages of the packaging of a microelectronic die according to one embodiment of the present invention. Referring more particularly to Fig. 2, a method according to one embodiment of the present invention involves starting from a bare ~~dielectric~~ wafer or substrate, such as a bare silicon wafer, and etching vias into the wafer, for example using laser beams, as depicted schematically by beams 10. The laser beams 10 create vias 14 in the

wafer, resulting in the initial die substrate shown in Fig. 2. It is to be noted that embodiments of the present invention include within their scope use of any other suitable ~~dielectric~~ material besides silicon, and of any other suitable methods of providing vias in silicon, as readily recognizable by one skilled in the art.

[0022] Referring now to Fig. 5, a schematic view is provided showing a silicon layer 20 as having been disposed on the layer of copper 18 of Fig. 4 to provide a dielectric-thermal conductor "sandwich" 22 according to one embodiment of the present invention. The dielectric layer 20 may include any dielectric material as would be within the knowledge of one skilled in the art, such as, for example, poly-silicon. By "~~dielectric~~ thermal conductor sandwich," what is meant in the context of embodiments of the present invention is that a thermal conductor, such as copper, is disposed between two ~~dielectric~~ layers, such as, as in the case of the embodiment shown in Figs 4 and 5, the layer of copper 18 sandwiched between the silicon layer 12 and the poly-silicon layer 20. The poly-silicon layer 20 may ~~comprise poly-silicon, having~~ have a sufficient thickness to allow conventional semi-conductor device pattern base layer and build up based on application needs. The poly-silicon layer 20 may, for example, measure between about 50 Angstroms to about 1 micron in thickness.

[0023] Referring next to Fig. 6, a schematic view is provided of an intermediate die 24 built up according to any one of standard manufacturing processes and incorporating the ~~dielectric~~-thermal conductor sandwich 22 shown in Fig. 5. The intermediate die 24 incorporates standard build up layers 26. The build up layers 26 may comprise any number of layers including signal and dielectric layers for providing a microelectronic circuit such as a microprocessor, as readily recognized by one skilled in the art. The building up of layers 26 takes place, according to embodiments of the present invention, upon a thermally conductive microelectronic die substrate, such as the ~~dielectric~~-thermal conductor sandwich shown in Fig. 5. By "thermally conductive microelectronic die substrate," what is meant in the context of embodiments of the present invention is a die substrate, such as a silicon wafer, on which a thermally conductive material is provided that allows the formation of thermal contact zones as shown by zones 28 in Fig. 7. According to the above definition, the substrate and layer of copper combination shown in Fig. 4 is also a thermally conductive microelectronic die substrate.

[0024] As seen in Fig. 7, according to one embodiment of the present invention, the intermediate die 24 of Fig. 6 is etched, prior to dicing for standard packaging, for exposing thermal contact zones 28 at the etched face of the die for providing a die 27. In the embodiment shown in Fig. 7, the thermal contact zones 28 comprise exposed parts of the copper layer 12

disposed in vias 14. The thermal contact zones allow a dissipation of heat from an inner region 30 of the die 27 away from the die. The etching may be effected using conventional atmospheric downstream plasma etching technology, although it is to be understood that other conventional methods may be used, as readily recognizable by one skilled in the art. As is well known, plasma etching is a process that utilizes an electrically excited gas to remove material from a device or unit. Selective plasma etching refers to a process that removes only specific materials, such as, in the case of the present invention as depicted in Figs. 2-9, removing only the silicon ~~dielectric~~ layer and not the layer of thermally conductive material.

[0027] As best seen in Fig. 9, the die package according to embodiments of the present invention allows for the placement of a plane of thermally conductive material, such as copper, very close, such as within a distance from about 1 micron to 2 microns, to the circuitry generating heat, such as circuit board 34. There is thus only a very thin silicon interface 20 through which heat must be conducted before it reaches the copper plane and is dissipated through the vias. The reduction of thermally isolating ~~dielectric~~ material between the circuitry and the heat spreader, and, in addition, the use of a direct thermal connection to the inner region of the die both work to improve heat dissipation away from the die.

[0028] Embodiments of the present invention are not limited to the

use of solder as a thermal interface material 38. Embodiments of the present invention further include within their scope the use of other thermal interface materials, such as, for example, organic thermal epoxy. While heat dissipation for a die package using organic thermal epoxy as the thermal interface material will be less than that for solder, the die package as a whole will exhibit a significant improvement in heat dissipation as compared with the use of thermal epoxy in die packages made according to prior art methods~~, where thermal epoxy is placed on a layer of silicon~~.

CONCLUSION

It is believed that a full and complete response has been made to the outstanding Notice of Non-Compliant Amendment. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Response is respectfully requested.

Respectfully submitted,

Intel Corporation

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I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below

By: Laleh Jalali Date: October 21, 2005